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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor: CHEN-KUEI CHUNG, ET AL.)
Application Serial No.: 10/057,025) Attorney Docket No.: IT0058-US
Filed: January 24, 2002)
Title: INTEGRATED MICRO-DROPLET)
GENERATOR)

**SUBMISSION OF REVOCATION OF POWER OF ATTORNEY
AND GRANT OF POWER OF ATTORNEY**

Assistant Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants hereby submit the attached Revocation of Power of Attorney and Grant of Power of Attorney in the above-identified application. Should there be any questions with respect to this submission a representative of the Patent Office is requested to contact the undersigned.

Respectfully submitted,

CHEN-KUEI CHUNG, ET AL.

Date: September 9, 2004

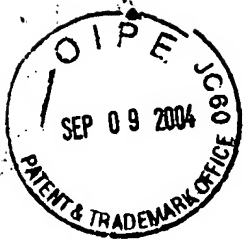
By:


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Customer No. 28970



PATENT
Customer No. 28970

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Patent Application and Patent Numbers: See attached "Schedule A"

REVOCATION OF POWER OF ATTORNEY
AND GRANT OF NEW POWER OF ATTORNEY

The undersigned, a representative authorized to sign on behalf of the assignee owning all of the interest in the listed and pending patent applications and issued patents on the attached sheet (Schedule A), hereby revokes all previous powers of attorney or authorization of agent granted in these patents before the date of execution hereof. The undersigned verifies that **INDUSTRIAL TECHNOLOGY RESEARCH INSTITUTE** is the assignee of the entire right, title, and interest in each of the pending patent applications and issued patents listed on the attached Schedule A and is identified as the assignee by assignments from the inventor(s) in the listed pending patent applications and issued patents as filed accordingly at the U.S. Patent and Trademark Office. The undersigned certifies that the evidentiary documents have been reviewed and to the best of the undersigned's knowledge and belief, title in each of the pending patent applications and issued patents listed on the attached Schedule A is in the assignee **INDUSTRIAL TECHNOLOGY RESEARCH INSTITUTE**.

By the undersigned's signature, **INDUSTRIAL TECHNOLOGY RESEARCH INSTITUTE** hereby grants power of attorney for each of the pending patent applications and issued patents listed on the attached Schedule A to **SHAW PITTMAN LLP**, Michael D. Bednarek, Reg. No. 32,329; Lawrence J. Gotts, Reg. No. 31,163; Aslan Baghdadi, Reg. No. 34,542; Yital Hu, Reg. No. 40,653; Elizabeth M. Roesel, Reg. No. 34,878; David C. Isaacson, Reg. No. 38,500; Steven P. Arnheim, Reg. No. 43, 475; Poh C. Chua, Reg. No. 44,615; Michael A. Oblon, Reg. No. 42,956; Lawrence D. Eisen, Reg. No. 41,009; Mark Koehn, Reg. No. 46,271; Michelle S. Marks, Reg. No. 41,971; Brett C. Martin, Reg. No. 52,000; Chad D. Wells, Reg. No. 50,875; Tara L. Hutchings, Reg. No. 46,559; John Kasha, Reg. No. 53,100; Ann P. McGeehan, Reg. No. 45,839; June E. Cohan, Reg. No. 43,741; and Joanne Kim, Reg. No. 51,193, both jointly and separately as its attorneys with full power of substitution and revocation, to transact all business in the Patent and Trademark Office connected with each of the pending patent applications and issued patents listed on the attached Schedule A.

Please send all future correspondence concerning the pending patent applications and issued patents listed on the attached Schedule A to SHAW PITTMAN LLP at the following address:

Shaw Pittman LLP
1650 Tysons Blvd.
McLean, Virginia 22102

Dated: 7/9, 2004

By: Alex Fan

Alex Fan
Director
IP Management & Legal Affairs Div./TTC
Industrial Technology Research Institute



SCHEDULE A

SERIAL NUMBER	FILING DATE	TITLE	PATENT NUMBER	ISSUE DATE
09/156,353	Sept. 18, 1998	Method for Forming Fine-Pitched Solder Bumps	6,268,114	July 31, 2001
09/634,556	Aug. 7, 2000	Method for Forming Electrically Conductive Bumps and Device Formed	6,767,818	July 27, 2004
09/822,533	March 30, 2001	Apparatus and Method for Etching Glass Panels	6,673,195	Jan. 6, 2004
09/846,643	May 1, 2001	Method for Forming a Wafer Level Package Incorporating a Multiplicity of Elastomeric Blocks and Package Formed	6,605,525	Aug. 12, 2003
09/864,013	May 23, 2001	Field Emission Display Panels Incorporating Cathodes Having Narrow Nanotube Emitters Formed on Dielectric Layers	6,750,604	June 15, 2004
10/004,920	Dec. 5, 2001	Method for Fabricating 3-Dimensional Solenoid and Device Fabricated	6,677,659	Jan. 13, 2004
10/032,523	Oct. 19, 2001	Liquid Crystal on Silicon Incorporating Integrated Spacers and Silicon Light Valves and Method for Fabrication	N/A	N/A
10/037,084	Dec. 31, 2001	Method for Fabricating a Tunable, 3-Dimensional Solenoid and Device Fabricated	6,621,139	Sept. 16, 2003
10/037,847	Oct. 19, 2001	Wide Viewing Angle Fringe Field Multi-Domain Aligned LCD and Method for Fabricating	N/A	N/A
10/038,994	Dec. 31, 2001	Microfluidic Mixer Apparatus and Microfluidic Reactor Apparatus for Microfluidic Processing	N/A	N/A
10/057,009	Jan. 24, 2002	Micro Fabrication with Vortex Shaped Spirally Topographically Tapered Spirally Patterned Conductor Layer and Method for Fabrication Thereof	6,734,074	May 11, 2004
10/057,025	Jan. 24, 2002	Integrated Micro-Droplet Generator	N/A	N/A
10/094,288	March 8, 2002	Method for Reducing Reactive ION Etching (RIE) Lag In Semiconductor Fabrication Processes	N/A	N/A
10/103,619	March 21, 2002	Fabry-Perot Filter Apparatus with Enhanced Optical Discrimination	6,768,555	July 27, 2004
10/152,468	May 21, 2002	Method for Bonding IC Chips to Substrates with Non-Conductive Adhesive and Assemblies Formed	6,605,491	Aug. 12, 2003
10/185,034	June 28, 2002	Method for Forming Amorphous Silicon Film on Single Crystal Silicon and Structure Formed	6,737,307	May 18, 2004

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10/190,276	July 5, 2002	Method for Bonding IC Chips to Substrates Incorporating Dummy Bumps and Non-Conductive Adhesive and Structures Formed	N/A	N/A
10/194,149	July 11, 2002	Method for Determining the Thermal Performance of a Heat Sink	6,663,278	Dec. 16, 2003
10/215,143	Aug. 8, 2002	Method for Fabricating an Integrated Nozzle Plate and Multi-Level Micro-Fluidic Devices Fabricated	N/A	N/A
10/233,802	Sept. 3, 2002	Wafer Level Package Incorporating Dual Complaint Layers and Method for Fabrication	N/A	N/A
10/236,271	Sept. 5, 2002	Microelectronic 3-D Solenoid of Circular Cross-Section and Method for Fabrication	N/A	N/A
10/236,608	Sept. 6, 2002	Method for Polysilicon Crystallization by Simultaneous Laser and Rapid Thermal Annealing	6,759,284	July 6, 2004
10/335,307	Dec. 31, 2002	Data Storage Device Utilizing Carbon Nanotubes and Method for Operating	N/A	N/A

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